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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WALTER, CRAIG E	
ART UNIT	**PAPER NUMBER**
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/786,250	SCHUBERT, RICHARD P.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *19-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I in the reply filed on 6 November 2006 is acknowledged. Applicant contends, "all three groups relate to the same general subject matter", and further asserts "all three groups recite a limitation involving "priority."". Applicant alleges for these reasons that the claims within each group are sufficiently related, and can and should be examined together. This traversal amounts to merely a general allegation that they claims are related, and uses very specific elements of select claims to justify their similarities. This argument is not persuasive as Examiner maintains that each invention was properly divided into groups that are in fact separate and distinct, and further reiterates that the three groups require a divergent search based on their respective subclasses within the 711 classification schedule. More specifically, Examiner has provided justification as why each invention is separate and distinct in the analysis provided in paragraph 0002 of the restriction requirement mailed on 3 October 2006, and further provided the proper classification of each group in order to justify a significant burden to Examiner to search each of these three separate inventions (see paragraph 0001 of the restriction requirement mailed on 3 October 2006). Applicant has not provided any specific arguments to address these assertions; therefore the requirement is still deemed proper and is therefore made FINAL. Claims 1-18 will be examined on the merits. Claims 19-30 are pending in the Application, but are withdrawn pursuant to Applicant's election of group I.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 21 June 2004 was fully considered by the examiner.

Drawings

3. The drawings were received on 25 February 2004. These drawings are deemed acceptable for examination.

Claim Objections

4. Claims 1-18 are objected to because of the following informalities:

As for claim 1, the phrase "the priority indicators" as recited in lines 6-7 of the claim should be changed to "priority indicators" to properly establish antecedent basis for the phrase.

As for claim 11, the phrase "item in t a pseudo" as recited in line 3 should be changed to "item in a pseudo" for clarity.

As for claim 15, the phrase "the first plurality of operations" as recited in lines 3-4 should be changed to "the first plurality of memory locations" to properly establish antecedent basis for the phrase.

Claims 2-10, 11-14 and 16-18 are objected to for inheriting the deficiency of claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 5-7 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Zangenehpour (US Patent 5,224,217).

As for claim 1, Zangenehpour teaches a method of operating a cache in a digital computer system, the cache having a plurality of memory locations, the method comprising:

a) obtaining a priority indicator with memory locations in the cache (col. 3, lines 23-44 – all memory locations are assigned a priority tag ranging from 0 to the total number of locations);

b) storing a new item in the cache by:

i) associating a priority with the new item (col. 3, lines 23-44 – highest priority tag is assigned to the newest entry);

ii) selecting a memory location in the cache based in part on the priority indicators of the memory locations in the cache relative to the priority of the new item (col. 3, lines 23-44 – lowest priority item is the first to be replaced);

iii) storing the new item in the selected memory location (col. 3, lines 23-44 – the newest entry is stored in the location from which the lowest priority item was recently purged);

c) associating the priority of the new item with the selected memory location in the cache (col. 3, lines 23-44 – again, highest priority is assigned to the newest entry).

As for claim 5, Zangenehpour teaches wherein selecting a memory location in cache based in part on the priority indicators comprises:

a) when the cache has an empty memory location suitable for storing the new item, storing the new item in an empty memory location (data needed is cached until the cache is full, then entries are replaced);

b) when the cache has no empty memory location suitable for storing the new item, storing the new item in the least recently used (LRU) memory location with a priority indicator that is the same or lower than the new item, if one exists, otherwise not storing the new item and treating the new item as not cacheable (col. 3, lines 23-44 – the newest entry is stored in the location from which the lowest priority item was recently purged).

As for claim 6, Zangenehpour teaches wherein selecting a memory location in cache based in part on the priority indicators comprises: storing the new item in the least recently used memory location with a priority indicator that is the same or lower than the new item, if one exists (col. 3, lines 23-44 – the newest entry is stored in the location from which the lowest priority item was recently purged).

As for claim 7, Zangenehpour teaches wherein selecting a memory location in cache based in part on the priority indicators comprises: storing the new item in the least recently used memory location with a priority indicator that is lower than the new item, if one exists (col. 3, lines 23-44 – the newest entry is stored in the location from which the lowest priority item was recently purged).

As for claim 12, Zangenehpour teaches the cache contains a data array and a tag array and associating a priority indicator with a memory location comprises storing a value in a field in the tag array (Fig. 2 – each cache frame contains data (element 32), and a tag (element 31), which contains the priority field - col. 4, lines 5-18).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-4, and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zangenehpour (US Patent 5,224,217) as applied to claim 1 above, and in further view of Tago et al. (US PG Publication 2002/0199091 A1), hereinafter Tago.

As for claims 2-4, 8-9, and 10-11, Zangenehpour teaches all of the elements of these claims (per the rejection of claims 5-7, 6-7, and 6-7 respectively), including assigning priorities based on an LRU policy. Zangenehpour however teaches neither

assigning priorities on a least frequently used (LFU), a least recently loaded policy, nor a pseudo random as recited in these claims.

Tago however teaches an apparatus for branch prediction based on history table in which he discusses cache eviction policies including LRU, FIFO (i.e. oldest or least recently loaded), and random in paragraph 0065, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Zangenehpour to further include Tago's apparatus into his own computer system using an LRU process for cache replacement. By doing so, Zangenehpour could exploit the benefits of utilizing a processor which performs its instruction branch predictions on a pattern history table, which could help to improve the prediction accuracy and minimize the amount of memory required by avoiding entry interference as taught by Tago in paragraphs 0014 through 0016, all lines.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zangenehpour (US Patent 5,224,217) as applied to claim 1 above, and in further view of Ozawa (US Patent 5,787,490).

As for claim 13, though Zangenehpour teaches all of the elements of claim 1, he fails to teach associating multiple processes with a priority, wherein the priority of the new item is derived from the priority of the process that generated the new item as recited in this claim.

Ozawa however teaches a multiprocess execution system that designates cache use priority based on process priority (col. 1, line 48 through col. 2, line 24 and abstract).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Zangenehpour to further include Ozawa's multiprocess execution system into his own computer system using an LRU process for cache replacement. By doing so, Zangenehpour could benefit from improved memory usage by ensuring that the highest priority process is not prevented from executing its preferential use, and further maximize process execution time as taught by Ozawa in col. 1, lines 17-45.

8. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zangenehpour (US Patent 5,224,217) as applied to claim 1 above, and in further view of Abe et al. (US Patent 5,906,000), hereinafter Abe.

As for claims 17 and 18, though Zangenehpour teaches all of the elements of claim 1, he fails to specifically teach storing the priority information in a table. Additionally, he fails to teach writing the priorities of the cache to a control register.

Abe however teaches a computer with a cache controller and cache memory with a priority table and priority levels which stores a priority table, used to record priorities of cache addresses in a control register (Fig. 5, elements 14 and 16 – col. 3, line 36 through col. 4, line 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Zangenehpour to further include Abe's computer system into his own computer system using an LRU process for cache replacement. By doing so, Zangenehpour could improve the speed of his cache by retaining data within the cache based on its access frequency as taught by Abe in col. 1, lines 19-42.

9. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zangenehpour (US Patent 5,224,217) as applied to claim 1 above, and in further view of Agarwala et al. (US Patent 6,484,237 B1), hereinafter Agarwala.

As for claims 14 and 15, Zangenehpour teaches:

a) assigning a first priority to a first portion of the plurality of memory locations (col. 3, lines 23-44 - the most recently used entry is given the highest priority);

b) assigning a second priority, lower than the first priority, to a second portion of the plurality of memory locations (col. 3, lines 23-44 - the most least used entry is given the lowest priority);

c) generating new items to store in the cache with priorities lower than or equal to the second priority (col. 3, lines 23-44 - the newest entry will be assigned a value equal to the priority of the second priority (i.e. highest)).

He fails however to teach using the first portion of the plurality of memory locations for non-cache memory operations, and a digital signal processor (DSP), which uses a portion for non-caching processor operations as recited in these claims.

Agarwala however teaches a unified multilevel memory system architecture which supports both cache and addressable SRAM, which utilizes a level one unified cache for both caching and instructions (i.e. non-caching) for a DSP - col. 2, lines 55-64.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Zangenehpour to further include Agarwala's unified memory system into

his own computer system using an LRU process for cache replacement. By doing so, Zangenehpour could improve the speed and effectiveness of his overall cache memory management by more effectively caching processor instructions and requests, as taught by Agarwala in col. 11, lines 18-49.

10. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Zangenehpour (US Patent 5,224,217) and Agarwala (US Patent 6,484,237 B1) as applied to claim 14 above, and in further view of Abe (US Patent 5,906,000).

As for claim 16, though the combined teachings of Zangenehpour and Agarwala teach all of the elements of claim 14, they fail to specifically teach writing the priorities of the cache to a control register.

Abe however teaches a computer with a cache controller and cache memory with a priority table and priority levels which stores a priority table, used to record priorities of cache addresses in a control register (Fig. 5, elements 14 and 16 – col. 3, line 36 through col. 4, line 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention for the combined teachings of Zangenehpour and Agarwala to further include Abe's computer system. By doing so, they could improve the speed of the cache by retaining data within the cache based on its access frequency as taught by Abe in col. 1, lines 19-42.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Sasaki et al. (US PG Publication 2003/0014603 A1) teach a cache control method and cache apparatus.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

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SUPERVISORY PATENT EXAMINER
1-10-07